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10/820,237	04/05/2004	Anatoliy V. Tsyrganovich	ZIL-519-1C	7465

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EXAMINER
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LIE, ANGELA M

ART UNIT	PAPER NUMBER
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2821

DATE MAILED: 01/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/820,237

Applicant(s)

TSYRGANOVICH, ANATOLIY V.

Examiner

Angela M. Lie

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 33-38, 40, 41 and 43-54 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 33-38, 40, 41, 43-47 and 50-54 is/are rejected.
- 7) ☒ Claim(s) 48 and 49 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 50 is objected to because of the following informalities: Language of claim 50 is unclear, the examiner does not understand what following phrase attempts to describe: "the first correction signal component varies parabolically over a portion of the first correction signal component". For the purposes of the examination, the examiner considers a correction signal to be parabolic. Appropriate correction is required.

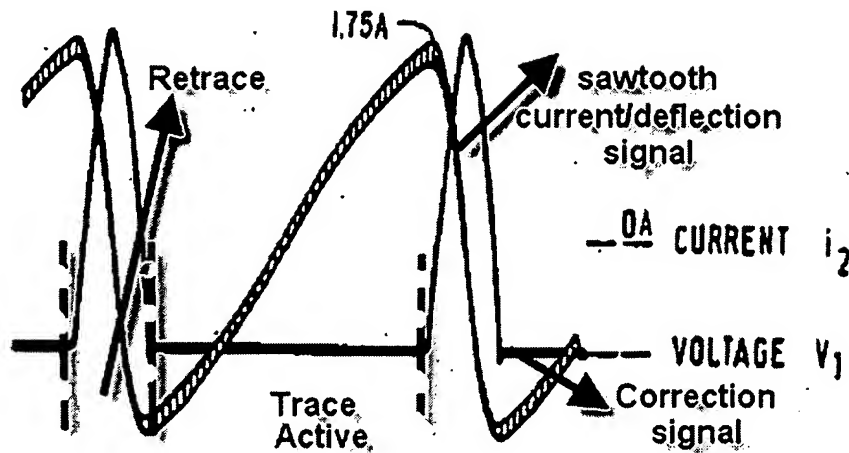
### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 33-37 and 44 are rejected under 35 U.S.C. 102(b) as being anticipated by Haferl (US Patent 4906902).



As to claim 34, Haferl discloses a horizontal deflection generator comprising: a circuit that generates a horizontal sawtooth signal having an amplitude (column 2, lines 61-62; and as shown in figure 1 above); and means for modulating the amplitude (column 1, lines 5-8) of the horizontal sawtooth signal (Figure 1 as indicated above) using a horizontal correction signal (Figure 1 as indicated above) to generate a horizontal deflection current signal, wherein the horizontal correction signal has a vertical active time  $t_{va}$  and a vertical retrace time  $t_{vr}$  (Figure 1 as indicated above), and wherein the horizontal deflection current signal is not distorted after a transition from the vertical active time  $t_{va}$  to the vertical retrace time  $t_{vr}$  (Figure 1, as shown above, during the times of transitions deflection current is not distorted), wherein the amplifier (column 1, lines 5-11, since the circuitry is capable of amplifying (changing an amplitude) the signal, it is equivalent with amplifier), wherein the means generates a modulated horizontal sawtooth signal (combination of generated sawtooth current and correction signal), and wherein the amplifier generates a modulated horizontal sawtooth signal, and wherein the amplifier generates the horizontal deflection current signal by

amplifying the modulated horizontal sawtooth signal (Haferl's circuit is capable of performing this function).

As to claim 33, Haferl discloses the horizontal deflection generator wherein the horizontal correction signal is a continuous signal (as shown in figure 1 above, the correction signal is continuous).

As to claim 35, Haferl discloses the horizontal deflection generator wherein the amplifier has a limited frequency bandwidth (column 1, lines 10-20; wherein amplification circuit comprises capacitor, and capacitor inherently has frequency limitation (i.e. does not pass high frequencies), therefore there inherently is a limited frequency bandwidth).

As to claim 36, Haferl discloses the horizontal deflection generator wherein the horizontal deflection generator is part of a raster display system (since Haferl teaches raster distortion corrected deflection circuit, it is inherent that similarly to other display circuitry, horizontal deflection generator is part of a raster display system).

As to claim 37, Haferl discloses the horizontal deflection generator wherein the horizontal deflection generator is implemented on a single integrated circuit device (column 3, lines 41-44).

As to claim 44, Haferl discloses a horizontal deflection generator comprising: a circuit that generates a horizontal sawtooth signal having an amplitude (column 2, lines 61-62; and as shown in figure 1 above); and means for modulating the amplitude of the horizontal sawtooth signal (column 1, lines 5-8) using a horizontal correction signal (Figure 1 as indicated above) to generate a horizontal deflection current signal, wherein

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the horizontal correction signal does not have any discontinuities (as shown in figure 1, the correction signal does not have any discontinuities) wherein the amplifier (column 1, lines 5-11, since the circuitry is capable of amplifying (changing an amplitude) the signal, it is equivalent with amplifier), wherein the means generates a modulated horizontal sawtooth signal (combination of generated sawtooth current and correction signal), and wherein the amplifier generates a modulated horizontal sawtooth signal, and wherein the amplifier generates the horizontal deflection current signal by amplifying the modulated horizontal sawtooth signal (Haferl's circuit is capable of performing this function).

4. Claims 40,41,45,46,47,50 and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Fernsler (US Patent 5034664).

As to claim 40, Fernsler teaches a circuit capable of performing a method comprising: generating a sawtooth signal, wherein the sawtooth signal has an amplitude (Figure 6, element 108); generating a correction signal (Figure 6, element 110), wherein the correction signal has a vertical retrace time  $t_{vr}$  and a vertical active time  $t_{va}$  (as shown in figure 6 below), wherein a circuit generates the correction signal, and wherein the circuit includes a level shifter (figure 6, element U4, wherein amplifier is capable of shifting the level of the signal; US Patent 4988927, column 4, lines 45-48) and an inverter (column 10, lines 1-2, if signal can be inverter, there inherently has to be an inverter); modulating the amplitude of the sawtooth signal using the correction signal to generate a deflection signal (since correction signal and sawtooth current are integrated together (Figure 6, element 100; the circuit taught by Fernsler is capable of modulating

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the amplitude of the sawtooth current); and amplifying the deflection signal to generate a deflection current signal (Figure 6, element U4), wherein the deflection current signal is not distorted when the correction signal transitions from the vertical retrace time  $t_{vr}$  to the vertical active time  $t_{va}$  (as shown in figure 6 below, furthermore the deflection current inherently can not be distorted when the correction signal transitions, because any discontinuity in the deflection signal would cause disturbance in a displayed image, and the device would not function properly).

As to claim 41, Fernsler teaches a circuit capable of performing a method comprising: generating a sawtooth signal, wherein the sawtooth signal has an amplitude (Figure 6, element 108); generating a correction signal (Figure 6, element 110), wherein the correction signal has a vertical retrace time  $t_{vr}$  and a vertical active time  $t_{va}$  (as shown in figure 6 below), wherein a circuit generates the correction signal, and wherein the circuit includes a level shifter (figure 6, element U4, wherein amplifier is capable of shifting the level of the signal; US Patent 4988927, column 4, lines 45-48) and a gain controller (column 9, line 68, and column 10, line 1); modulating the amplitude of the sawtooth signal using the correction signal to generate a deflection signal (since correction signal and sawtooth current are integrated together (Figure 6, element 100; the circuit taught by Fernsler is capable of modulating the amplitude of the sawtooth current); and amplifying the deflection signal to generate a deflection current signal (Figure 6, element U4), wherein the deflection current signal is not distorted when the correction signal transitions from the vertical retrace time  $t_{vr}$  to the vertical active time  $t_{va}$  (as shown in figure 6 below, furthermore the deflection current inherently can not be

distorted when the correction signal transitions, because any discontinuity in the deflection signal would cause disturbance in a displayed image, and the device would not function properly).

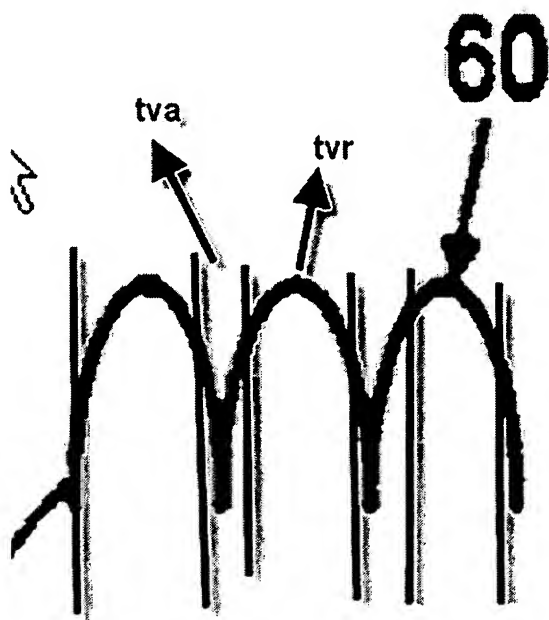


Figure 6

As to claim 45, Fernsler discloses the method wherein the sawtooth signal is a horizontal sawtooth signal (Figure 6, element 108), and wherein the correction signal is a horizontal correction signal (Figure 6, element 110).

As to claim 46, Fernsler discloses the method wherein generating the correction signal comprises generating a higher-order signal (Figure 4, element 60, parabola is a higher order signal (not linear i.e.  $x^2$ )).

As to claims 47 and 51, Fernsler discloses the method wherein generating the correction signal is performed by combining a first correction signal component with a second correction signal component (as shown in figure 4) such that the correction



signal has no discontinuities (Figure 4, element 60, parabolic correction signal is a continuous signal).

As to claim 50, Fersnler discloses the correction signal having a parabolic shape (as shown in figure 4, element 60).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 38,43 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haferl (US Patent 4906902) in the view of Pspice (<http://www.orcad.com/pspicead.aspx>).

As to claim 38, Haferl teaches a horizontal deflection generator comprising: a circuit that generates a horizontal sawtooth signal having an amplitude (column 2, lines 61-62; and as shown in figure 1 above); and means for modulating the amplitude (column 1, lines 5-8) of the horizontal sawtooth signal (Figure 1 as indicated above) using a horizontal correction signal (Figure 1 as indicated above) to generate a horizontal deflection current signal, wherein the horizontal correction signal has a vertical active time tva and a vertical retrace time tvr (Figure 1 as indicated above), and wherein the horizontal deflection current signal is not distorted after a transition from the vertical active time tva to the vertical retrace time tvr (Figure 1, as shown above, during the times of transitions

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deflection current is not distorted). He does not teach, that the horizontal deflection generator is implemented in software, however such programs as PSpice used for circuit simulation are well known in the art since 1985

(<http://www.orcad.com/pspicead.aspx>), therefore it would have been obvious to one of the ordinary skill in the art during the time the invention was made to implement horizontal deflection circuit as taught by Haferl in the software such as Pspice, because Pspice allows to reflect true signal analysis, without spending money on the expensive circuit parts, furthermore if circuitry does not function properly it is also easier for the designer to find a faulty connection thanks to signal graphs and measurements which can be taken at any node.

As to claim 43, Haferl discloses a horizontal deflection generator comprising: a circuit that generates a horizontal sawtooth signal having an amplitude (column 2, lines 61-62; and as shown in figure 1 above); and means for modulating the amplitude of the horizontal sawtooth signal (column 1, lines 5-8) using a horizontal correction signal (Figure 1 as indicated above) to generate a horizontal deflection current signal, wherein the horizontal correction signal does not have any discontinuities (as shown in figure 1, the correction signal does not have any discontinuities). He does not teach, that the horizontal deflection generator is implemented in software, however such programs as PSpice used for circuit simulation are well known in the art since 1985

(<http://www.orcad.com/pspicead.aspx>), therefore it would have been obvious to one of the ordinary skill in the art during the time the invention was made to implement horizontal deflection circuit as taught by Haferl in the software such as Pspice, because

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Pspice allows to reflect true signal analysis, without spending money on the expensive circuit parts, furthermore if circuitry does not function properly it is also easier for the designer to find a faulty connection thanks to signal graphs and measurements which can be taken at any node.

As to claim 52, Haferl teaches the horizontal deflection generator wherein the horizontal deflection generator is part of a computer display (column 2, line 56, wherein television and computer display are functionally equivalent).

As to claim 53, Haferl teaches a horizontal deflection generator, wherein the horizontal correction signal has no discontinuities (as shown in figure 1 above, the correction signal is continuous).

As to claim 54, Haferl teaches the horizontal deflection generator wherein the horizontal deflection generator is implemented on a single integrated circuit device (column 3, lines 41-44).

#### ***Allowable Subject Matter***

7. Claims 48 and 49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter:

As to claim 48, the prior art of record fails to teach the method as discloses in claim 47, wherein the first correction signal component has a constant amplitude during the vertical active time tva.

As to claim 49, the prior art of record fails to teach the method as discloses in claim 47, wherein the first correction signal component has a constant amplitude during the vertical retrace time tvr.

### ***The Prior Art***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US Patent 5583400 discloses a deflection correction circuit comprising horizontal waveform generator, a vertical waveform generator, an integrator and an amplifier.
- US Patent 5596250 discloses a deflection waveform correction circuit comprising: horizontal sawtooth signal, a correction signal and an amplifier.


### ***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angela M. Lie whose telephone number is 571-272-8445. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Angela M Lie

  
WILSON LEE  
PRIMARY EXAMINER